17.2 A Passive UHF RFID Tag LSI with 36.6% Efficiency CMOS-Only Rectifier and Current-Mode Demodulator in 0.35µm FeRAM Technology

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Although RFID tag LSIs storing only unique IDs have been developed to minimize costs [1][2], the costs of both the tag fabrication and attaching it to products are even higher than the cost of the tag LSI itself, restricting their applicability. Tags with rewritable memory can enhance system performance, security, and cost-effectiveness by reducing transactions between reader/writer (R/W) and host computer. This paper illustrates primary design techniques for developing a passive UHF RFID tag LSI with 2kb FeRAM for the rewritable tag. A CMOS full-wave rectifier can improve the efficiency from 16.6% [3] up to 36.6% by means of lossless internal V_{th} cancellation and asymmetrical stack architecture. A current-mode ASK demodulator converts the 15% power modulation into a linear current signal over a 27dB dynamic range of the incoming power. The resulting FeRAM-based tag has a communication range that is identical for both read and write operations, and a 32b read-and-write operation for each tag can be executed at a rate of 129 tags/s. These features cannot be achieved by EEPROM technology.

Figure 17.2.1 shows a block diagram of the developed tag LSI. A CMOS full-wave rectifier (CFR) generates the internal supply voltage VDD from a UHF carrier from a R/W. A booster generates the 3V FeRAM supply, and over-current protection (OCP) suppresses maximum applied voltages below the breakdown voltage for the maximum 4W EIRP R/W output. Even if RF power shuts off during FeRAM access, data integrity is assured by the ferroelectric smoothing capacitor, which supplies the necessary energy for FeRAM access. The ferroelectric capacitor can reduce chip size since its permittivity is 10 times larger than an oxide capacitor. ASK power modulation from the R/W is detected as a current change in the CFR, and the current-mode demodulator (CMD) converts it into voltage form, and sends it to the logic block. The minimum modulation index to be detected is 15%. The CMD also adjusts the internal VCO clock frequency from an incoming fixed-frequency preamble. The logic block accesses the FeRAM according to the decoded command, and generates response data. The modulator transmits an FM0 coded signal by changing the tag backscatter amplitude.

Figure 17.2.2 compares the half-wave rectifier units used in conventional NMOS [3] and the proposed CMOS full-wave rectifiers. The maximum communication range of a passive RFID tag depends on the rectifier efficiency and power consumption of the tag LSI. To improve the efficiency, the input parasitic capacitance (C_p) and the threshold voltage (V_{th}) drop in the MOS diodes used in the rectifier should be minimized, since C_p forms a leakage path between the antenna terminals and V_{th} reduces the generating VDD. The conventional NMOS rectifier unit reduces the influence from the V_{th} drop by applying an external bias voltage V_{bth} pre-charged to C_b between the gate and source terminals. However, this configuration, degrades the efficiency due to the additional parasitic capacitances C_{p2} and C_{p3} of the switch transistors associated with C_b. The CFR removes the influences from C_{p2} and C_{p3} by separating C_b from the input terminal N_1 with a pMOS diode M_{p1}. The input capacitor C_{inF} is a ferroelectric capacitor, which can reduce the area and C_p. The internal V_{th} cancellation circuit can compensate for the process and temperature variation in V_{th} by matching M_{pb}-M_{p1} and M_{nb}-M_{n1}. The leakage currents in all diodes are negligibly small due to the large bias resistances R_b.

Figure 17.2.3 compares architectures of the conventional [3] and the proposed full-wave rectifiers. The conventional architecture achieves voltage multiplication by the stack of three-stage half-wave rectifier units. Since this structure is symmetrical around the antenna terminals, the influence of C_p appears for both ANT+ and ANT- terminals. The proposed design has a mirror stack structure of CMOS half-wave rectifier units to optimize power efficiency rather than voltage multiplication ability. The ANT- terminal is connected to the folded node of the mirror stack, and operates as AC ground. As a result, the parasitic capacitance at the ANT- node does not degrade the efficiency. D_1 and D_2 are bypass diodes to clamp the ANT+ voltages against a large current pulse. These diodes contribute to minimizing the CFR area and C_p, and improve the ESD voltage.

Figure 17.2.4 shows characteristics for both rectifiers. The efficiency of the proposed CFR is 36.6% at 953MHz, which is 2.1 times higher than the conventional NMOS full-wave rectifier. The area of the CFR is reduced to 0.08 times thanks to the ferroelectric capacitors and mirror stack architecture.

Figure 17.2.5 compares the ASK demodulation principles in the conventional voltage-sensing method [4] with the current-sensing method used here. Conventionally, ASK demodulation at high incoming power has been a design concern since the over-current protection diminishes the signal voltage. The current-sensing method enables the modulation power to be converted into a linear current change for the entire communication range and suppresses the operation voltage far below the device breakdown voltage. From measurements, the current linearity is observed over a 27dB dynamic range of the input power, as shown in Fig. 17.2.5.

Figure 17.2.6 shows the block diagram of the CMD. The input current of the CMD, I_{ASK}, is obtained from the current signal in the CFR, I_{CFR}, by removing the UHF carrier component in the LPF. The current peak hold circuit detects the maximum value of I_{ASK}, and its output, I_{PK}, is used to create current signal I_{SIG} ($=I_{PK}-I_{ASK}$) and reference I_{REF} ($I_{PK}\times\alpha$). The current comparator is a transimpedance amplifier to generate the NRZ voltage signal. Measured results at maximum input power condition are shown in Fig. 17.2.6. The CMD successfully generates the voltage signal with sufficient SNR. This architecture is suitable for low-voltage operation since the adopted current processing is independent of the supply voltage.

Figure 17.2.7 shows the die micrograph and summary of the tag LSI characteristics. The LSI is fabricated in 0.35µm CMOS FeRAM technology, and the die size is 1.23×1.50mm^2. The operating air interface, protocol, and commands are compliant to ISO/IEC 18000-6. The ESD voltage between antenna terminals is over 3,000V for the Human Body Model (HBM). The communication range is 0m–4.3m at 4W EIRP for both read and write operations, and the throughput of 32b read-and-write operation for each tag is 129 tags/s, which is 2.9 times higher than for an EEPROM-based tag LSI.

References:

[1] M. Usami et al., "Powder LSI: An Ultra Small RF Identification Chip for Individual Recognition Applications," *ISSCC Dig. Tech. Papers*, pp. 398-399, Feb., 2003.

[2] XRA00, "UHF, EPCglobal Class1b, Contactless Memory Chip", STMicroelectronics, Data Sheet, 2004.

[3] T. Umeda et al., "A 950MHz Rectifier Circuit for Sensor Networks with 10m-Distance," *ISSCC Dig. Tech. Papers*, pp. 256-257, Feb., 2005.

[4] U. Karthaus et al., "Fully Integrated Passive UHF RFID Transponder IC With 16.7-µW Minimum RF Input Power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602-1608, Oct., 2003.

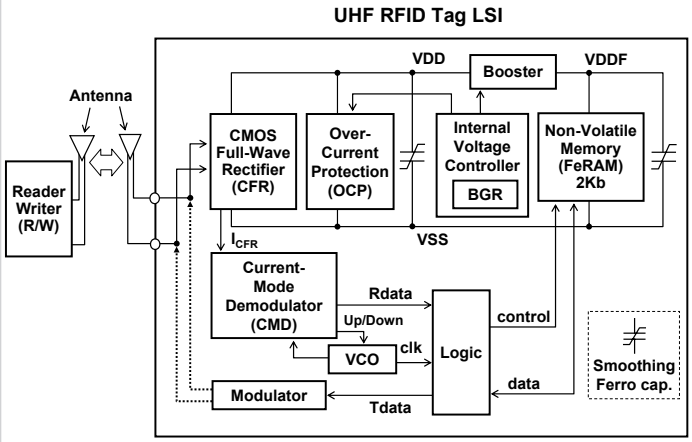


Figure 17.2.1: Block diagram of the UHF RFID tag LSI with 2Kb FeRAM.

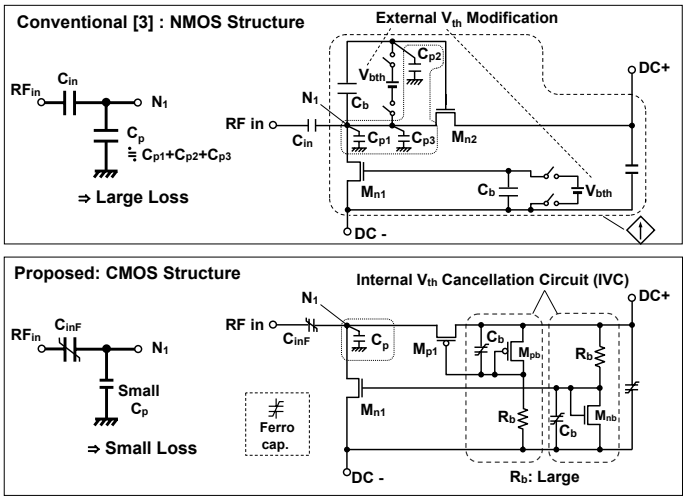


Figure 17.2.2: Comparison of the conventional and the proposed half-wave rectifier units.

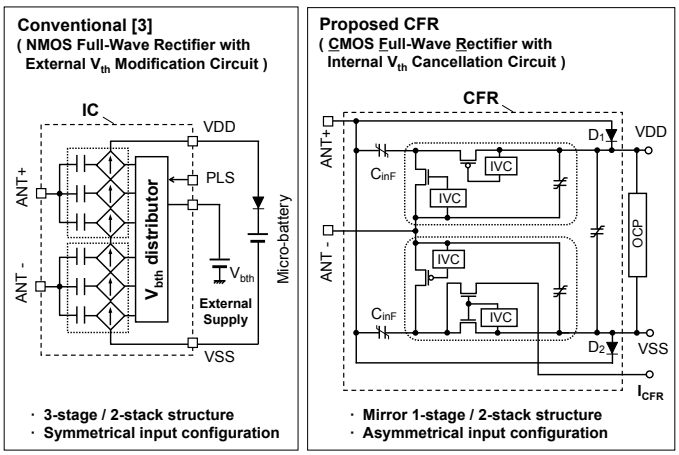
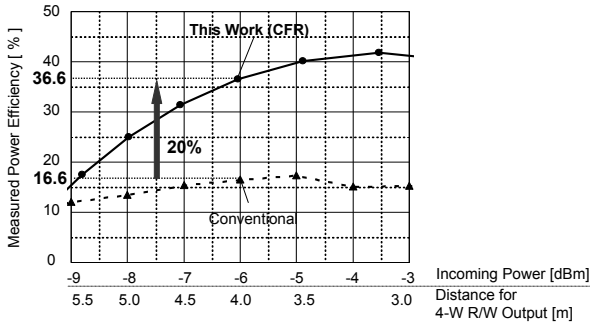


Figure 17.2.3: Comparison of architectures for the conventional and proposed full-wave rectifiers.



		This Work (CFR)	Conventional [3]	Ratio
Measured Efficiency [%]	@ 4m / 953MHz	**36.6**	16.6	**2.1**
	@ 5m / 953MHz	**25.0**	13.5	**1.8**
Circuit Area [mm^2]		**0.008**	0.104	**0.08**
Condition	Technology	0.35μm	0.30μm	
	Number of stacks	2	2	
	Number of stages	1	3	

Figure 17.2.4: Characteristics of full-wave rectifiers.

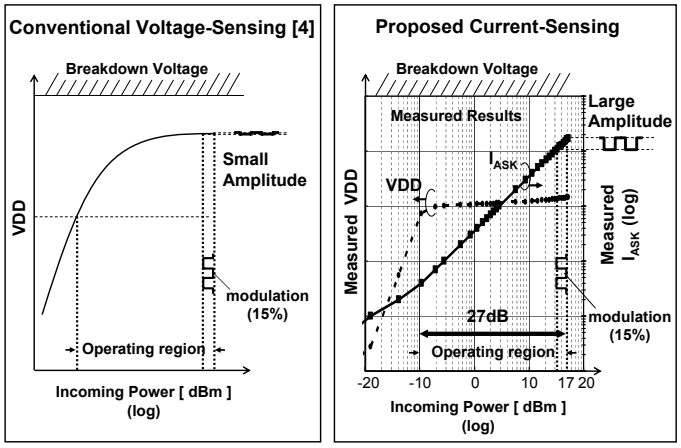


Figure 17.2.5: The demodulation principles of the voltage-sensing and current-sensing methods.

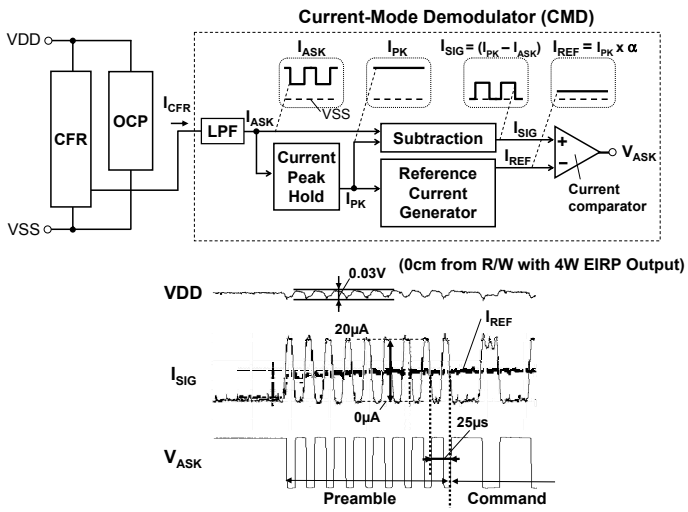


Figure 17.2.6: The block diagram and measured results of CMD circuit.

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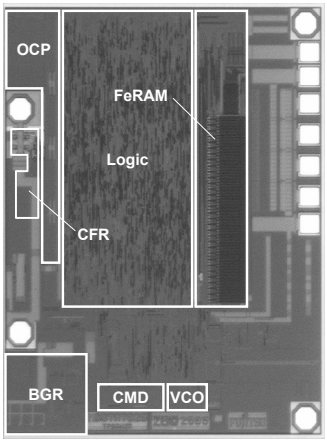

Operation Frequency	860MHz - 960MHz
Modulation (Forward)	ASK
Modulation Index (Forward)	15% (Minimum)
Data Rate (Forward)	10/40kb/s
Modulation (Return)	Backscatter Amplitude
Data Rate (Return)	40/160kb/s
FeRAM Capacity	2kb
ESD Protection (HBM)	3,000V
Communication Range (4W EIRP)	Read: 0m - 4.3m Write: 0m - 4.3m
Inventory Throughput	~100tags/s
Read/Write Throughput	129tags/s
Technology	0.35μm CMOS FeRAM
Die Size	1.23mm x 1.5mm

Figure 17.2.7: Die micrograph of the tag LSI.

